We claim:

1. A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising:

a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

a register file coupled to the data path and containing a plurality of registers; and

an execution unit coupled to the data path, the execution unit configurable to perform a group instruction that operates on a plurality of data elements in partitioned fields of a register to produce a catenated result, the execution unit further configurable to execute:

(i) an aligned instruction operable to copy first data according to an aligned memory address, the first data having a data width, the data width specified as a fixed value by the aligned instruction, the aligned memory address being one of a plurality of memory addresses regularly spaced at alignment boundaries separated by the data width; and

(ii) an unaligned instruction operable to copy second data according to an unaligned memory address, the second data having the data width, the data width specified as a fixed value by the unaligned instruction, the second data being permitted to cross an alignment boundary of the data width, the unaligned memory address being a memory address that is not constrained to be one of the plurality of memory addresses regularly spaced at alignment boundaries separated by the data width.

2. The system of claim 1 wherein the aligned instruction comprises a load instruction operable to copy the first data from memory at the aligned memory address to a register, and the unaligned instruction comprises a load instruction operable to copy the second data from memory at the unaligned memory address to a register.

3. The system of claim 1 wherein the aligned instruction comprises a store instruction operable to copy the first data from a register to memory at the aligned memory address, and the unaligned instruction comprises a store instruction operable to copy the second data from a register to memory at the unaligned memory address.

4. The system of claim 1 wherein the group instruction is capable of operating on data having a data width of 128 bits.

5. The system of claim 1 wherein the group instruction is a group floating-point instruction.

6. The system of claim 1 wherein the group instruction is a group integer instruction.

7. The system of claim 1 wherein the aligned instruction and the unaligned instruction are capable of accessing the first data and the second data, each having the data width of 128 bits

8. The system of claim 1 wherein the aligned instruction and the unaligned instruction are capable of accessing the first data and the second data, each having the data width of 64 bits.

9. The system of claim 1 wherein the plurality of regularly spaced memory addresses are separated by intervals of 128 bits.

10. The system of claim 1 wherein the plurality of regularly spaced memory addresses are separated by intervals of 64 bits.

11. The system of claim 1 wherein the aligned instruction responds by generating an exception if the aligned memory address is not one of a plurality of memory addresses regularly spaced at alignment boundaries separated by the data width.

12. The system of claim 1 wherein the execution unit is further configurable to execute two aligned instructions in parallel using hardware capable of executing a single unaligned instruction.

13. The system of claim 1 wherein the aligned instruction corresponds to a first binary code and the unaligned instruction corresponds to a second binary code, the first binary code matching the second binary code in all but one bit position.

14. A computer-readable medium having instructions that cause a computer to perform operations, the instructions comprising:

an instruction that operates on a plurality of data elements in partitioned fields of at least one register to produce a catenated result;

an aligned instruction operable to copy first data according to an aligned memory address, the first data having a data width, the data width specified as a fixed value by the aligned instruction, the aligned memory address being one of a plurality of memory addresses regularly spaced by the data width; and

an unaligned instruction operable to copy second data according to an unaligned memory address, the second data having the data width, the data width specified as a fixed value by the unaligned instruction, the unaligned memory address being a memory address that is not constrained to be one of the plurality of memory addresses regularly spaced by the data width.

15. The computer-readable medium of claim 14 wherein the aligned instruction comprises a load instruction operable to copy the first data from memory at the aligned memory address to a register, and the unaligned instruction comprises a load instruction operable to copy the second data from memory at the unaligned memory address to a register.

16. The computer-readable medium of claim 14 wherein the aligned instruction comprises a store instruction operable to copy the first data from a register to memory at the aligned memory address, and the unaligned instruction comprises a store instruction operable to copy the second data from a register to memory at the unaligned memory address.

17. The computer-readable medium of claim 14 wherein the group instruction is capable of operating on data having a data width of 128 bits.

18. The computer-readable medium of claim 14 wherein the group instruction is a group floating-point instruction.

19. The computer-readable medium of claim 14 wherein the group instruction is a group integer instruction.

20. The computer-readable medium of claim 14 wherein the aligned instruction and the unaligned instruction are capable of accessing the first data and the second data, each having the data width of 128 bits

21. The computer-readable medium of claim 14 wherein the aligned instruction and the unaligned instruction are capable of accessing the first data and the second data, each having the data width of 64 bits.

22. The computer-readable medium of claim 14 wherein the plurality of regularly spaced memory addresses are separated by intervals of 128 bits.

23. The computer-readable medium of claim 14 wherein the plurality of regularly spaced memory addresses are separated by intervals of 64 bits.

24. The computer-readable medium of claim 14 wherein the aligned instruction responds by generating an exception if the aligned memory address is not one of a plurality of memory addresses regularly spaced at alignment boundaries separated by the data width.

25. The computer-readable medium of claim 14 wherein two aligned instructions are capable of parallel execution.

26. The computer-readable medium of claim 14 wherein the aligned instruction corresponds to a first binary code and the unaligned instruction corresponds to a second binary code, the first binary code matching the second binary code in all but one bit position.

27. A computer data signal, embodied in a transmission medium, the computer data signal having instructions that cause a computer to perform operations, the instructions comprising:

an instruction that operates on a plurality of data elements in partitioned fields of at least one register to produce a catenated result;

an aligned instruction operable to copy first data according to an aligned memory address, the first data having a data width, the data width specified as a fixed value by the aligned instruction, the aligned memory address being one of a plurality of memory addresses regularly spaced by the data width; and

an unaligned instruction operable to copy second data according to an unaligned memory address, the second data having the data width, the data width specified as a fixed value by the unaligned instruction, the unaligned memory address being a memory address that is not constrained to be one of the plurality of memory addresses regularly spaced by the data width.

28. The computer data signal of claim 27 wherein the aligned instruction comprises a load instruction operable to copy the first data from memory at the aligned memory address to a register, and the unaligned instruction comprises a load instruction operable to copy the second data from memory at the unaligned memory address to a register.

29. The computer data signal of claim 27 wherein the aligned instruction comprises a store instruction operable to copy the first data from a register to memory at the aligned

memory address, and the unaligned instruction comprises a store instruction operable to copy the second data from a register to memory at the unaligned memory address.

30. The computer data signal of claim 27 wherein the group instruction is capable of operating on data having a data width of 128 bits.

31. The computer data signal of claim 27 wherein the group instruction is a group floating-point instruction.

32. The computer data signal of claim 27 wherein the group instruction is a group integer instruction.

33. The computer data signal of claim 27 wherein the aligned instruction and the unaligned instruction are capable of accessing the first data and the second data, each having the data width of 128 bits

34. The computer data signal of claim 27 wherein the aligned instruction and the unaligned instruction are capable of accessing the first data and the second data, each having the data width of 64 bits.

35. The computer data signal of claim 27 wherein the plurality of regularly spaced memory addresses are separated by intervals of 128 bits.

36. The computer data signal of claim 27 wherein the plurality of regularly spaced memory addresses are separated by intervals of 64 bits.

37. The computer data signal of claim 27 wherein the aligned instruction responds by generating an exception if the aligned memory address is not one of a plurality of memory addresses regularly spaced at alignment boundaries separated by the data width.

38. The computer data signal of claim 27 wherein two aligned instructions are capable of parallel execution.

39. The computer data signal of claim 27 wherein the aligned instruction corresponds to a first binary code and the unaligned instruction corresponds to a second binary code, the first binary code matching the second binary code in all but one bit position.